App # 09/899,093

Draft Amendment

Claim 1.

A method of driving a passive matrix addressed display or memory array of cells comprising an electrically polarizable ferroelectric material exhibiting hysteresis, wherein the polarization state of individual, separately addressable cells can be switched to a desired condition by application of electric potentials or voltages to corresponding word and bit lines in said passive matrix, the method comprising the steps of:

controlling individually a potential on selected word and bit lines to approach or coincide with one of n predefined potential levels, ~~wherein n ≥ 3~~, the potentials on said selected word and bit lines forming subsets of said n predefined potentials involving n_{WORD} and n_{BIT} potentials, respectively;

controlling the potentials on all word- and bit lines in a time-coordinated fashion according to a protocol or timing sequence, whereby word lines are latched in a predetermined sequence to potentials selected among the n_{WORD} potentials, while bit lines are either latched in a predetermined sequence to potentials selected among the n_{BIT} potentials or are connected during a certain period of the timing sequence to sensing circuitry that senses charges flowing between at least one cell

and its associated the bit line, to form a crossline voltage potential between bit lines and word lines; and

arranging said timing sequence to encompass at least two distinct parts, including a read cycle during which charges flowing between a said selected bit line and the cells connecting to said bit line as sensed by the sensing circuitry, and a refresh/write cycle during which polarization state(s) in cells connecting with selected word- and bit lines are controlled to correspond with a set of predetermined values, where the word and bit lines include a first crossline voltage potential between an unselected bit line and a selected word line, a second crossline voltage potential between a selected bit line and an unselected word line, and a third crossline voltage potential between an unselected bit line and an unselected word line, the sum of the first, second and third crossline voltage potentials being less than or substantially equal to Vs ~~the timing sequence results in unselected bit lines and word lines having an average a crossline voltage potential ≤ Vs/3,~~ during read/write cycles, where Vs is the voltage across an addressed cell during read, refresh, and write cycles,

wherein all memory locations are accessed solely by its corresponding bit and word line on a single array layer.